MULTISTAGE DIGITAL CROSS CONNECT WITH INTEGRAL FRAME TIMING

ABSTRACT OF THE DISCLOSURE

A digital cross connect comprises plural switching stages. Each stage has plural switches which receive plural frames of time multiplexed input data and which switch

5   the data in time and space. Configurations of the switches change in frame synchronization at the start of a synchronized data frame. Both the configuration data and a frame clock may be propagated through the plural stages from a master switch. First and last stages of the digital cross connect may be implemented on common chips having two framing time bases. Data may be aligned to a global frame clock and

10   interchanged using a single random access memory in a time slot interchanger. The write address to the random access memory is generated from a local frame counter keyed to the input data frame while a read address is transformed from a global frame counter.